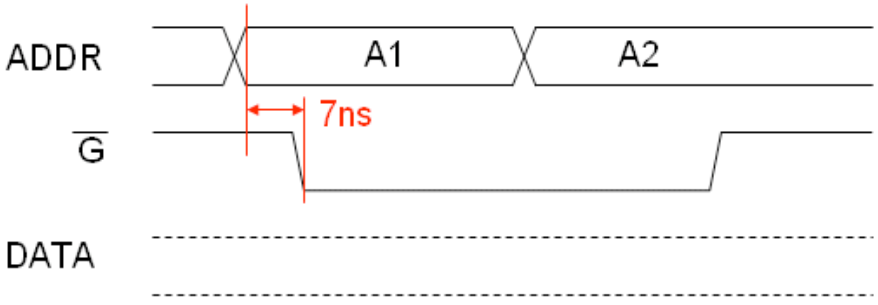
M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2008

Lecture PSet #7
Due: Tue, 09/30/08

Problem 1. The Motorola MCM6264 integrated circuit is a 8Kx8 static RAM. When answering the following questions about the timing of its various signals please refer to the data sheet (http://web.mit.edu/6.111/www/f2008/handouts/6264.pdf). Assume you are using the -12 version of the MCM6264.

(A) The timing diagram below shows two READ accesses, one for location A1 and the other for location A2. Complete the timing diagram, drawing a detailed plot of the DATA signal showing where it is high impedance, changing and stable. Annotate your diagram with times derived from the data sheet. Assume that the chip's enable signals (E1bar, E2) are asserted. Note that the output enable signal (G) goes low 7ns after the address has become stable. Your timings should reflect that information.



(B) The timing diagram below shows a single WRITE access. Complete the timing diagram, drawing a detailed plot of the DATA signal showing when it must be valid with respect to the write enable (Wbar) control signal. Anotate your diagram with times derived from the data sheet, showing the necessary timing relationships between ADDR, Wbar and DATA. Assume that the chip's enable signals (E1bar, E2) are asserted and that the output enable (Gbar) is deasserted.